

FET

FET.. Field effect Transistor

→ The Current Flow between the two terminal (Source S & Drain D) is controlled by an electric field applied to the third terminal (Gate G).

→ FET is called (Unipolar) because current depends only on majority carriers (E or h) = one carrier only. while NPN or PNP depends on 2 carriers.

Advantages & disadvantages of FET compared to BJT

- 1- FET is Voltage controlled current source Device (VCCS) while BJT is current controlled current source ~ (CCCS).
- 2- FET has large i/p impedance, so it is preferred than BJT as input stage to multistage amplifier.
- 3- FET generates lower noise level than BJT.
- 4- FET more Temperature stable than BJT.
- 5- FET is easier to be fabricated than BJT.
- 6- FET acts as VCR (voltage controlled resistor)

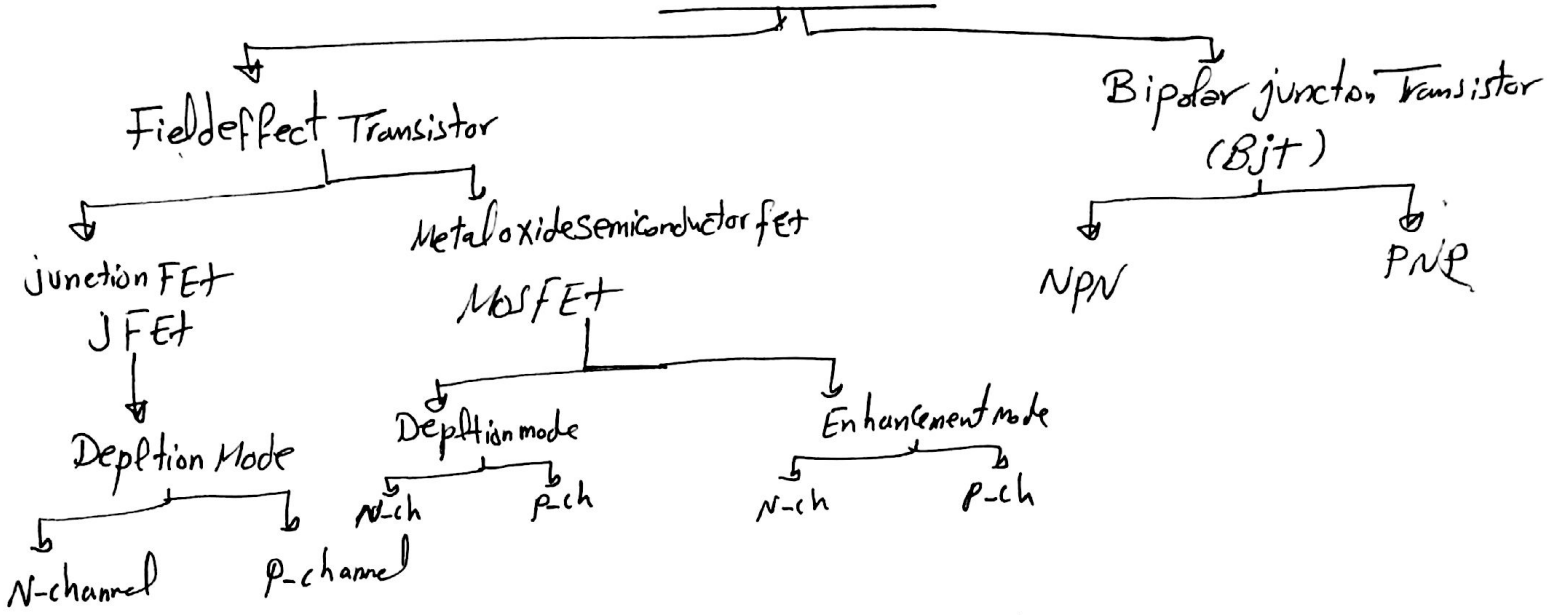
disadvantages

- 1- FET has poor frequency response (low BW)
- 2- Poor linearity (non linear relation between I_D, V_{GS})
- 3- Due to static charges → Damage occurred.

→ Uses of FET → Flash memory, USB drive, Camera, laptop, CPU, -- etc

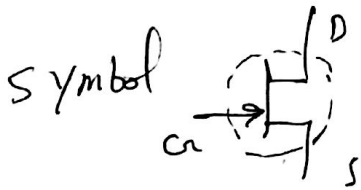
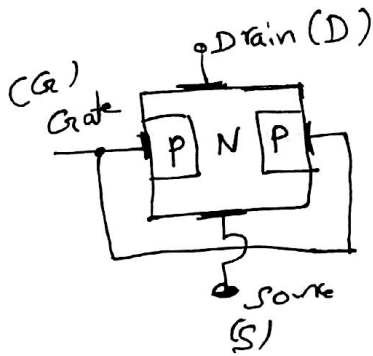
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Transistor Family

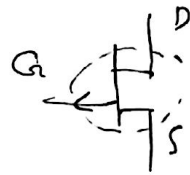
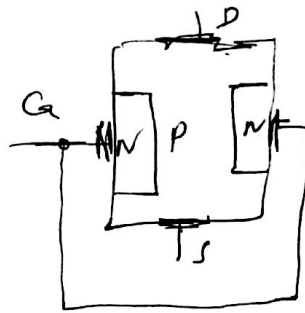


1 JFET (Junction Field effect Transistor)

1- N-channel



2- P-channel



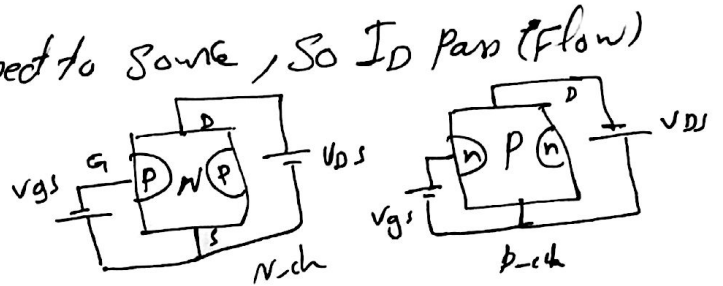
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- it is a 3 terminals semiconductor devices, The current conduction by one type of carriers (Electrons, holes)

- uses of FET more than BJT. (Nowadays)

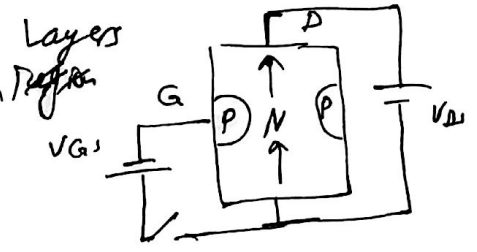
Notes (operation of JFET)

- [1] The voltage between gate and source (gate reverse biased)
- [2] The input circuit (gate-to-source) of JFET is reverse biased ∴ device has high input impedance.
- [3] The drain is so biased with respect to source, so I_D pass (flow) from source to drain.
- [4] in All JFETs, $I_S = I_D$



Working

- [1] The two PN junction at the sides form depletion regions. The current conduction by charge carriers (free electrons) flow through the channel between the 2 depletion layers & out of the drain.
- [2] the width of this channel (Resistance) can be controlled by changing the input voltage (V_{GS})
 if $V_{GS} \uparrow \rightarrow$ depletion region (wider) \rightarrow conduction channel (narrower)
- [3] JFET operates on principle that width of hence Resistance of conducting channel can be varied by changing V_{GS}



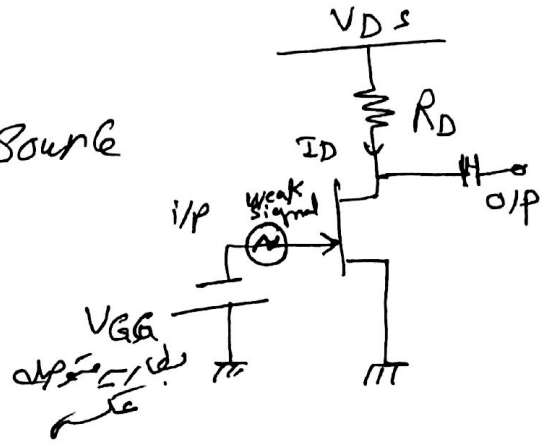
OR [the magnitude of Drain current I_D changed by V_{GS}]

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

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JFET as amplifier

* a weak signal applied between gate & source & amplified output obtained in the Drain source circuit.



* V_{GS} reverse connected with weak signal

* A small change in the reverse bias on gate \rightarrow produce large change in I_D .

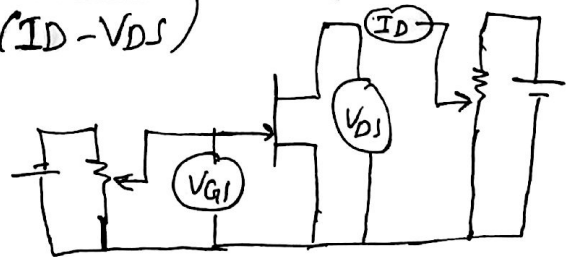
1. * During ^{negative} ~~positive~~ half cycle of the signal, the reverse voltage on gate increases & I_D decreases \rightarrow The result is small change in voltage at the gate large change in drain current. (I_D)

2. * during positive half cycle \rightarrow The reverse bias on gate decrease this increase channel width & increase drain current.

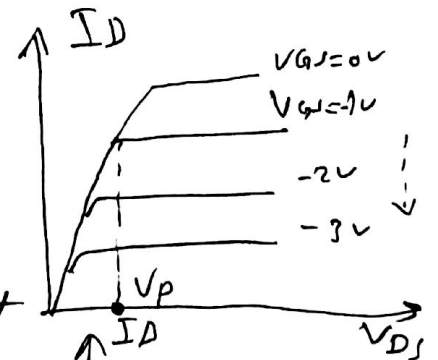
3. * Now, large variation of drain current \rightarrow produce output across load $R_D \rightarrow$ so FET act as an amplifier

output characteristics of JFET ($I_D - V_{DS}$)

* Firstly, I_D increased rapidly with $V_{DS} \uparrow$ but then become constant. (where $V_{DS} = V_p$ pinchoff)



* after V_{DS} increased than V_p , the channel width become narrow, depletion region touch each other, I_D pass through small area between these layers \therefore The increase of I_D is very small with ($V_{DS} > V_p$) $\therefore I_D$ remains constant



(JFET) \approx μ

